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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,570	12/31/2003	Mikko Waltari	109822-98	8972

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EXAMINER	
WAMSLEY, PATRICK G	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,570	WALTARI, MIKKO	
	Examiner	Art Unit	
	Patrick G. Wamsley	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4,7-12,14-16 and 18-21 is/are rejected.

7)☒ Claim(s) 3,5,6,13 and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/22/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: -- Variable Clock Rate Analog-to-Digital Converter Using a Delay Locked Loop --.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,154,164 to Gross, hereafter Gross.

Gross discloses a variable clock rate analog-to-digital converter, hereafter ADC. Specifically, Gross provides a clock generation circuit [114] able to produce a number of clock signals [116 / 118 / 120 / 122] having different clock periods [col. 2, line 13].

For claim 15, as shown in Table 1, Gross indicates that longer settling times are needed for more significant bits, hereafter MSBs, while shorter settling times are needed for less significant bits, hereafter LSBs. Therefore, as shown in Table 2, having various duration clock cycles [col. 7, line 25], Gross uses longer cycles for MSBs and shorter cycles for LSBs.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4, 7-12, 16, and 18-21, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art, hereafter APA, in view of Gross.

For claim 1, APA provides an algorithmic ADC [Page 2, ¶3] comprising a sample-and-hold circuit clocked by a sampling clock having a substantially uniform clock period [Page 3, ¶4]. While the exact words "sample-and-hold" are not used, it is clear that conventional algorithmic ADCs contain such circuits, as applicant discloses a combination of "sampling" [Page 2, ¶3] a continuous analog signal and then quantizing it. Because every clock pulse has an equal length [Page 3, ¶4], APA's sampling clock must have a substantially uniform clock period.

Unlike claim 1, APA lacks an internal ADC clock having at least two clock cycles with different lengths. In contrast, Gross provides a clock generation circuit [114] able to produce a number of clock signals [116 / 118 / 120 / 122] having different clock periods [col. 2, line 13]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied the clock teachings of Gross to APA's ADC. The motivation would have been to improve the speed of conversion, as suggested by Gross [col. 1, lines 36-37].

Independent claims 11 and 18 restate these apparatus limitations in method format. Independent claim 16 restates these apparatus limitations in means plus function format.

APA satisfies the additional limitations of independent claim 18 by providing a residue voltage [Page 3, ¶3], combined with the reference voltage [Page 2, ¶3] to produce another residue voltage, equivalent to the recited "intermediate analog voltage." This process continues for N bits, repeating for each clock cycle until it reaches the LSB [Page 3, ¶3]. Feedback signals are inherently present because APA uses a recirculating ADC [Page 2, ¶3].

For claims 2, 12, and 21, as shown in Table 1, Gross indicates that longer settling times are needed for MSBs, while shorter settling times are needed LSBs. Therefore, as shown in Table 2, having various duration clock cycles [col. 7, line 25], Gross uses longer cycles for MSBs and shorter cycles for LSBs.

For claim 4, recirculating ADCs [Page 2, ¶3] inherently include MDACs, due to their cyclical nature. APA's ADC must have a structure similar to prior art Fig. 1b in U.S. Patent 6,501,411 to Soundarapandian et al, a sub-ADC [102] coupled to a [MDAC]. Such elements are required for proper operation of a multi-stage ADC, due to the repeated use of residue voltages [Page 3, ¶3].

For claims 7-10, Gross discloses that a variable clock rate ADC may be used in a microprocessor, microcontroller, digital signal processor, or as a stand-alone converter [col. 7, lines 58-61]. Microprocessors comprise video encoders and decoders. Stand-alone converters can be found in set top boxes and electronic appliances.

For claim 19, the use of switched capacitor circuits [Page 10, ¶44] in ADCs is conventional. Applicant admits "any type" of low latency ADC [Page 10, ¶44] can be used, so it is evident that this step is part of APA. Moreover, the reference and residue voltages [Pages 2-3, ¶3] must inherently be applied to switched capacitors during each conversion cycle.

For claim 20, recirculating ADCs [Page 2, ¶3] inherently use feedback signals, applying them during each successive cycle to determine a reference voltage.

Allowable Subject Matter

Claims 3, 5-6, 13, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious the use of a delay locked loop, hereafter DLL, to generate an internal ADC clock having at least two cycles of different length [for claims 3, 13, and 17]; integration of sample / hold and MDAC circuits [for claims 5 and 6]. APA's DLL uses identical delay elements [Page 22, ¶85] instead of having multiple delay elements with different delay values.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,826,247 describes a phase locked loop, hereafter PLL, having a digital DLL. U.S. Patent 6,794,912 to Hirata et al provides a clock generator [10] and multiple delay circuits [40 / 60 / 80].

U.S. Patent 6,700,523 to Konno provides a sample / hold circuit [102] for an ADC. U.S. Patent 6,680,634 to Ruha et al describes a digital DLL. U.S. Patent 6,541,952 to Nagaraj couples sample / hold circuits [102a / 102b] to ADCs [106 / 108]. U.S. Patent 6,486,820 to Allworth et al discloses an ADC having a sample / hold circuit [409]. U.S. Patent 5,886,562 to Garrity et al synchronizes clock signals for an ADC. U.S. Patent 5,796,358 to Shih et al shows an ADC decoder [625] coupled to a sample / hold circuit [615]. U.S. Patent 4,893,124 to Tsuji et al shows an ADC with sample / hold circuits [15a / 15b] and delay circuits [16 / 18].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick G. Wamsley whose telephone number is (571) 272-1814. The official facsimile number is (703) 872-9306. An alternate facsimile number, (571) 273-1814, should only be used for unofficial documents.

Patrick G. Wamsley
April 7, 2005